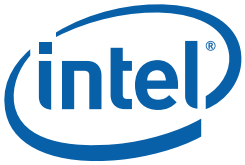

Intel® Atom™ Processor Z5xx[Δ] Series

Datasheet

Intel® Atom™ Processor Z540[Δ], Z530[Δ], Z520[Δ], Z510[Δ], and Z500[Δ] on 45 nm process technology

April 2008

Document Number: 319535-001US

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Revision History

Revision Number	Description	Revision Date
-001	• Initial release	April 2008

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1 Introduction

The Intel® Atom™ processor Z5xx series is built on a new 45-nanometer Hi-k low power micro-architecture and 45 nm process technology — the first generation of low-power IA-32 micro-architecture specially designed for the new class of Mobile Internet Devices (MIDs). In the Intel® Centrino® Atom™ processor technology platform, the Intel® Atom™ processor Z5xx series supports the Intel® System Controller Hub (Intel SCH), a single-chip component design for low-power. This document contains electrical, mechanical and thermal specifications for the following processors:

- Intel® Atom™ processor Z540, Z530, Z520, Z510, and Z500

Note: In this document, Intel® Atom™ processor Z5xx series refers to the Intel® Atom™ processor Z540, Z530, Z520, Z510, and Z500

Note: In this document, the Intel® Atom™ processor Z5xx series is referred to as “processor”. The Intel System Controller Hub (Intel SCH) is referred to as “Intel SCH”.

1.1 Major Features

The following list provides some processor key features:

- New single-core processor for mobile devices offering enhanced performance
- On die, primary 32-kB instructions cache and 24-kB write-back data cache
- 100-MHz and 133-MHz Source-Synchronous front side bus (FSB)
  - 100 MHz: Intel® Atom™ processor Z500
  - 133 MHz: Intel® Atom™ processor Z540, Z530, Z520, and Z510
- Supports Hyper-Threading Technology 2-threads
- On die 512-kB, 8-way L2 cache
- Support for IA 32-bit architecture
- Intel® Virtualization Technology (Intel® VT)
- Intel® Streaming SIMD Extensions 2 and 3 (Intel® SSE2 and Intel® SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Supports new CMOS FSB signaling for reduced power
- Micro-FCBGA8 packaging technologies
- Thermal management support using TM1 and TM2
- FSB Lane Reversal for flexible routing
- Supports C0/C1(e)/C2(e)/C4(e)
- Intel® Deep Power-Down Technology (C6)
- L2 Dynamic Cache Sizing
- New Split-V_{TT} support for lowest processor power state
- Advanced power management features including Enhanced Intel SpeedStep® Technology
- Execute Disable Bit support for enhanced security

1.2 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a non-maskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as address or data), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level).
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the Intel SCH component).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
CMOS	Complementary metal-Oxide semiconductor.
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to low power devices.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
Intel® Virtualization Technology (Intel® VT)	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
TDP	Thermal Design Power
V_{CC}	The processor core power supply
VR	Voltage Regulator
V_{SS}	The processor ground

Term	Definition
V_{CC}HFM	V_{CC} at Highest Frequency Mode (HFM).
V_{CC}LFM	V_{CC} at Lowest Frequency Mode (LFM).
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up.
V_{CCP}	AGTL+ Termination Voltage.
V_{CCPC6}	AGTL+ Termination Voltage.
V_{CCA}	PLL Supply voltage.
$V_{CCDPPWDN}$	V_{CC} at Deep Power-Down Technology (C6).
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep (C4).
V_{CCF}	Fuse Power Supply.
I_{CCDES}	I_{CCDES} for Intel® Atom™ processor Z5xx series Recommended Design Target power delivery (Estimated).
I_{CC}	I_{CC} for Intel® Atom™ processors Z5xx series is the number that can be use as a reflection on battery life estimates.
$I_{AH,}$	I_{CC} Auto-Halt
I_{SGNT}	I_{CC} Stop-Grant.
I_{DSLP}	I_{CC} Deep Sleep.
$dI_{CC/dt}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin (Estimated).
I_{CCA}	I_{CC} for V_{CCA} Supply.
P_{AH}	Auto Halt Power.
P_{SGNT}	Stop Grant Power.
P_{DPRSLP}	Deeper Sleep Power.
P_{DC6}	Deep Power-Down Technology (C6).
T_J	Junction Temperature.

1.3 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1. References

Document	Document Number/Location
Intel® System Controller Hub (Intel® SCH) Datasheet	319537
Intel® Atom™ Processor Z5xx Series Specification Update	319538
Intel® 64 and IA-32 Architectures Software Developer's Manuals *Volume 1: Basic Architecture* *Volume 2A: Instruction Set Reference, A-M* *Volume 2B: Instruction Set Reference, N-Z* *Volume 3A: System Programming Guide* *Volume 3B: System Programming Guide*	http://www.intel.com/products/processor/manuals/index.htm
AP-485, Intel® Processor Identification and CPUID Instruction Application Note	http://www.intel.com/design/processor/applnots/241618.htm

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2 Low Power Features

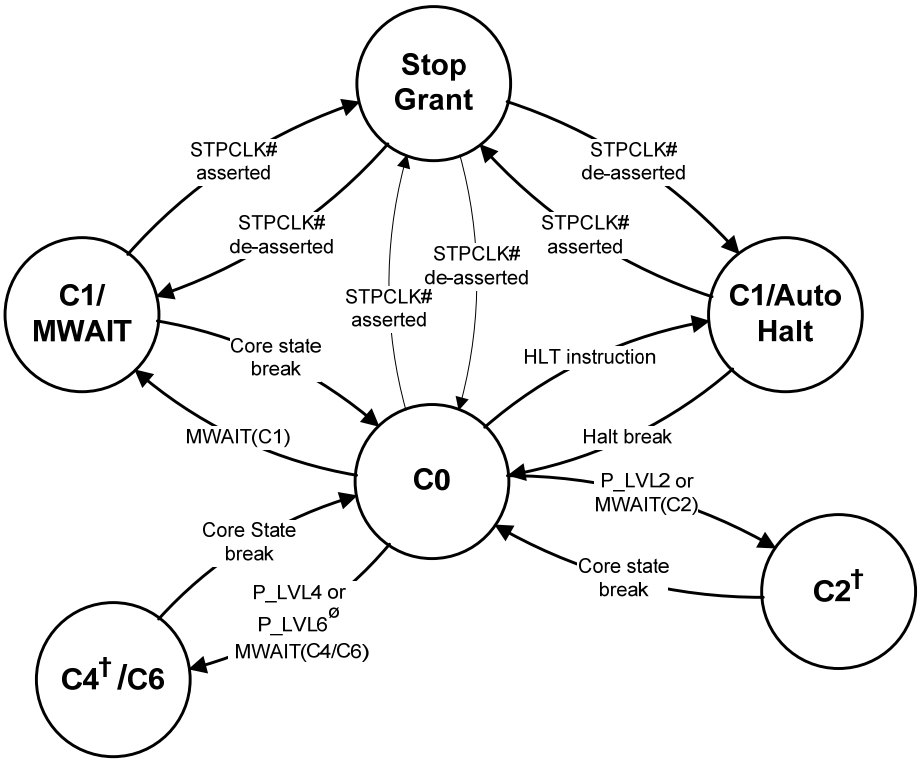
2.1 Clock Control and Low-power States

The processor supports low power states at the thread level and the core/package level. Thread states (TCx) loosely correspond to ACPI processor power states (Cx). A thread may independently enter the TC1/AutoHALT, TC1/MWAIT, TC2, TC4 or TC6 low power states, but this does not always cause a power state transition. Only when both threads request a low-power state (TCx) greater than the current processor state will a transition occur. The central power management logic ensures the entire processor enters the new common processor power state. For processor power states higher than C1, this would be done by initiating a P_LVLx (P_LVL2 and P_LVL3) I/O read to the chipset by both threads. Package states are states that require external intervention and typically map back to processor power states. Package states for processor include Normal (C0, C1), Stop Grant and Stop Grant Snoop (C2), Deeper Sleep (C4), and Deep Power-Down Technology (C6).

The processor implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads on the processor FSB. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured in a software programmable MSR by BIOS. If a thread encounters a chipset break event while STPCLK# is asserted, then it asserts the PBE# output signal. Assertion of PBE# when STPCLK# is asserted indicates to system logic that individual threads should return to the C0 state and the processor should return to the Normal state.

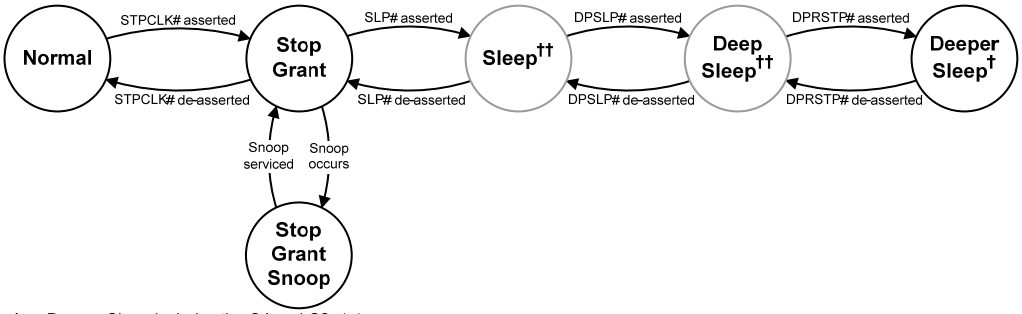
Figure 1 shows the thread low-power states. Figure 2 shows the package low-power states. Table 2 provides a mapping of thread low-power states to package low power states.

Figure 1. Thread Low-Power States



halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, RESET#, SMI#, or APIC interrupt
core state break = (halt break OR Monitor event) AND STPCLK# high (not asserted)
† — STPCLK# assertion and de-assertion have no effect if a core is in C2 or C4.
Ø — P_LVL6 read is issued once the L2 cache is reduced to zero.

Figure 2. Package Low-Power States



† — Deeper Sleep includes the C4 and C6 states
†† — Sleep and Deep Sleep are not states directly supported by the processor, but rather sub-states of the processor's C4/C6

Table 2. Coordination of Thread Low-Power States at the Package Level/Core Level

Thread 0 / Thread 1	TC0	TC1[1]	TC2	TC4/TC6
TC0	Normal (C0)	Normal (C0)	Normal (C0)	Normal (C0)
TC1[1]	Normal (C0)	AutoHalt (C1)	AutoHalt (C1)	AutoHalt (C1)
TC2	Normal (C0)	AutoHalt (C1)	Stop-Grant (C2)	Stop-Grant (C2)
NOTES: TC4/TC6	Normal (C0)	AutoHalt (C1)	Stop-Grant (C2)	Deeper Sleep (C4) /Deep Power-Down (C6)

NOTE: [1] AutoHALT or MWAIT/C1.

NOTE: To enter a package/core state, both threads must share a common low power state. If the threads are not in a common low power state, the package state will resolve to the highest common power C state.

2.1.1 Package/Core Low-Power State Descriptions

The following state descriptions assume that both threads are in a common low power state. For cases when only one thread is in a low power state no change in power state will occur.

2.1.1.1 Normal State (C0, C1)

This is the normal operating state for the processor. The processor remains in the Normal state when the processor/core is in the C0, C1/AutoHALT, or C1/MWAIT state. C0 is the active execution state.

2.1.1.1.1 C1/AutoHalt Powerdown State

C1/AutoHALT is a low-power state entered when one thread executes the HALT instruction while the other is in the TC1 or greater thread state. The processor will transition to the C0 state upon occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt messages. RESET# will cause the processor to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Powerdown state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Powerdown state. When the system de-asserts the STPCLK# interrupt, the processor will return to the HALT state.

While in AutoHALT Powerdown state, the processor will process bus snoops. The processor will enter an internal snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the AutoHALT Powerdown state.

2.1.1.1.2 C1/MWAIT Powerdown State

C1/MWAIT is a low-power state entered when one thread executes the MWAIT(C1) instruction while the other thread is in the TC1 or greater thread state. Processor behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor to return to the C0 state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set Reference, A-M* and *Volume 2B: Instruction Set Reference, N-Z*, for more information.

2.1.1.2 C2 State

Individual threads of the dual-threaded processor can enter the TC2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C2) instruction. Once both threads have C2 as a common state, the processor will transition to the C2 state; however, the processor will not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted by the chipset.

While in the C2 state, the processor will process bus snoops. The processor will enter a snoopable sub-state described the following section (and shown in Figure 1), to process the snoop and then return to the C2 state.

2.1.1.2.1 Stop-Grant State

When the STPCLK# pin is asserted, each thread of the processors enters the Stop-Grant state within 1384 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle. When the STPCLK# pin is de-asserted, the core returns to its previous low-power state.

Since the AGTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to V_{CCP}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

RESET# causes the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. When RESET# is asserted by the system, the STPCLK#, SLP#, DPSLP#, and DPRSTP# pins must be de-asserted prior to RESET# de-assertion. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be de-asserted after the de-assertion of SLP#.

While in Stop-Grant state, the processor will service snoops and latch interrupts delivered on the FSB. The processor will latch SMI#, INIT#, and LINT[1:0] interrupts and will service only one of each upon return to the Normal state.

The PBE# signal may be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt or Monitor event latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that the entire processor should return to the Normal state.

A transition to the Stop-Grant Snoop state occurs when the processor detects a snoop on the FSB (see Section 2.1.1.2.2). A transition to the Sleep state (see Section 2.1.1.3.1) occurs with the assertion of the SLP# signal.

2.1.1.2.2 Stop-Grant Snoop State

The processor responds to snoop or interrupt transactions on the FSB while in Stop-Grant state by entering the Stop-Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. The processor returns to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

2.1.1.3 C4 State

Individual threads of the processor can enter the C4 state by initiating a P_LVL4 I/O read to the P_BLK or an MWAIT(C4) instruction. Attempts to request C3 will also covert to C4 requests. If both processor threads are in C4, the central power management logic will request that the entire processor enter the Deeper Sleep package low-power state using the sequence through the Sleep and Deep Sleep states all described in the following sections.

To enable the package level Intel Enhanced Deeper Sleep state, Dynamic Cache Sizing and Intel Enhanced Deeper Sleep state fields must be configured in the PMG_CST_CONFIG_CONTROL MSR. Refer to Section 2.1.1.3.3 for further details on Intel Enhanced Deeper Sleep state.

2.1.1.3.1 Sleep State

The Sleep state is a low-power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and stops all internal clocks. The Sleep state is entered through assertion of the SLP# signal while in the Stop-Grant state and is only a transition state for Intel Atom™ processor Z5xx series. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertion while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP#, or RESET#) are allowed on the FSB while the processor is in Sleep state. Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior. Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be de-asserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin (see Section 2.1.1.3.2). While the processor is in the Sleep state, the SLP# pin must be de-asserted if another asynchronous FSB event needs to occur.

2.1.1.3.2 Deep Sleep State

The Deep Sleep state is entered through assertion of the DPSLP# pin while in the Sleep state and is also only a transition state for the Intel® Atom™ processor Z5xx series. BCLK may be stopped during the Deep Sleep state for additional platform level power savings. As an example, BCLK stop/restart timings on appropriate chipset-based platforms with the CK540 clock chip are as follows:

- **Deep Sleep entry:** the system clock chip may stop/tristate BCLK within 2 BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.
- **Deep Sleep exit**: the system clock chip must start toggling BCLK within 10 BCLK periods within DPSLP# de-assertion.

To re-enter the Sleep state, the DPSLP# pin must be de-asserted. BCLK can be re-started after DPSLP# de-assertion as described above. A period of 15 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin must be de-asserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in Deep Sleep state. When the processor is in Deep Sleep state, it will not respond to interrupts or snoop transactions. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.1.1.3.3 Deeper Sleep State

The Deeper Sleep state is similar to the Deep Sleep state, but further reduces core voltage levels. One of the potential lower core voltage levels is achieved by entering the base Deeper Sleep state. The Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep state. The following lower core voltage level is achieved by entering the Intel Enhanced Deeper Sleep state which is a sub-state of Deeper Sleep state. Intel Enhanced Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep only when the L2 cache has been completely shut down. Refer to Section 2.1.1.3.4 for further details on reducing the L2 cache and entering Intel Enhanced Deeper Sleep state.

In response to entering Deeper Sleep, the processor drives the VID code corresponding to the Deeper Sleep core voltage on the VID[6:0] pins.

Exit from Deeper Sleep or Intel Enhanced Deeper Sleep state is initiated by DPRSTP# de-assertion when the core requests a package state other than C4 or the core requests a processor performance state other than the lowest operating point.

2.1.1.3.4 Intel® Atom™ Processor Z5xx Series C5

As mentioned previously in this document, each C state has latency and transitory power costs associated with entering/exiting idle states. When the processor is interrupted, it must awake to service some request(s). If these requests occur at a high frequency, it is possible that more power will be consumed entering/exiting the states than will be saved. To alleviate this concern, the Intel Atom™ processor Z5xx series implements a new state called 'Intel Atom™ processor Z5xx series C5'. The Intel Atom™ processor Z5xx series C5 is not exposed to software. The only way to enter the C5 state is using a hardware promotion of C4 (with the cache ways shrunk to zero).

When the processor is in C4, the chipset assumes the processor has data in its cache. Often, the processor has fully flushed its cache. To avoid waking up the processor to service snoops when there is no data in its caches, the processor will automatically promote C4 requests to C5 (when the cache is flushed). The chipset treats C5 as a non-snoopable state. Therefore, all snoops will be completed from the I/O DMA masters without waking up the processor.

While similar, the Intel Atom™ processor Z5xx series C5 differs from the Core 2 Duo T5000/T7000 C5 implementation. In the Intel Atom™ processor Z5xx series C5, the V_{CC} will not be powered below the retention of caches voltage; there is no need to initialize the processor's caches on a C5 exit, and C5 is not architecturally enumerated to software. This state is the same as the Intel Atom™ processor Z5xx series's C5.

2.1.1.4 C6 State

C6 is a new low power state being introduced on the Intel Atom™ processor Z5xx series. C6 behavior is the same as Intel Enhanced Deeper Sleep with the addition of an on-die SRAM. This memory saves the processor state allowing the processor to lower its main core voltage closer to 0 V. It is important to note that V_{CC} cannot be lower while only 1 thread is in C6 state.

The processor threads can enter the C6 state by initiating a P_LVL6 I/O read to the P_BLK or an MWAIT(C6) instruction. To enter C6, the processor's caches must be flushed. The primary method to enter C6 used by newer operating systems (that support MWAIT) will be through the MWAIT instruction.

When the thread enters C6, it saves the processor state that is relevant to the processor context in an on-die SRAM that resides on a separate power plane V_{CCP} (I/O power supply). This allows the core V_{CC} to be lowered to any arbitrary voltage including 0 V. The microcode performs the save and restore of the processor state on entry and exit from C6 respectively.

To improve the amount of power reduction possible in the Deep Power-Down Technology state, a split V_{TT} is implemented. See Section 2.5.1 for additional information.

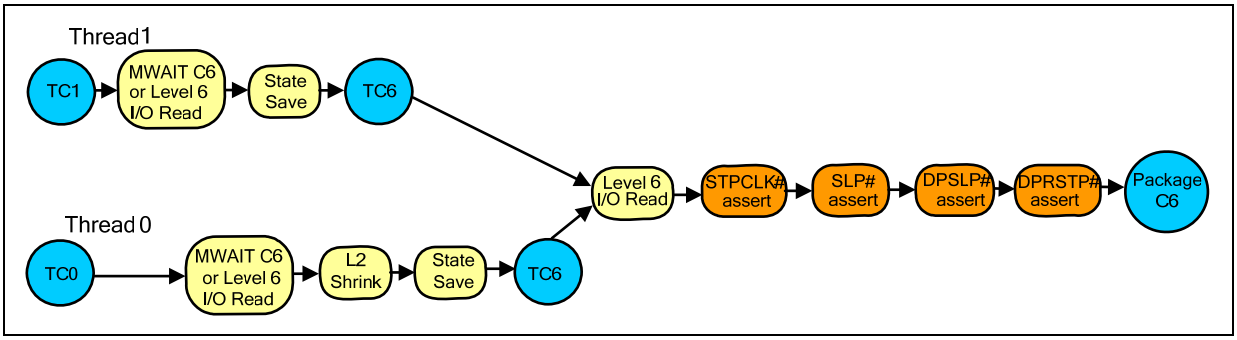
2.1.1.4.1 Intel® Deep Power-Down Technology State (Package C6 State)

When both threads have entered the C6 state and the L2 cache has been shrunk down to zero ways, the processor will enter the Deep Power-Down Technology state. To do so, the processor saves its architectural states in the on-die SRAM that resides in the V_{CCP} domain. At this point, the core V_{CC} will be dropped to the lowest core voltage closer to 0.3 V. The processor is now in an extremely low-power state. While in this state, the processor does not need to be snooped as all the caches were flushed before entering the C6 state.

The Deep Power-Down Technology exit sequence is triggered by the chipset when it detects a break event. It de-asserts the DPRSTP#, DPSLP#, SLP#, and STPCLK# pins to return to C0. At DPSLP# de-assertion, the core V_{CC} ramps up to the LFM value and the processor starts-up its internal PLLs. At SLP# de-assertion the processor is reset and the architectural state is read back into the threads from an on-die SRAM.

Refer to Figure 3 and Figure 4 for Deep Power-Down Technology entry sequence and exit sequences.

Figure 3. Deep Power-Down Technology Entry Sequence



NOTE: Deep Power-Down Technology is referred to as C6 in the above figure.

Figure 4. Deep Power-Down Technology Exit Sequence

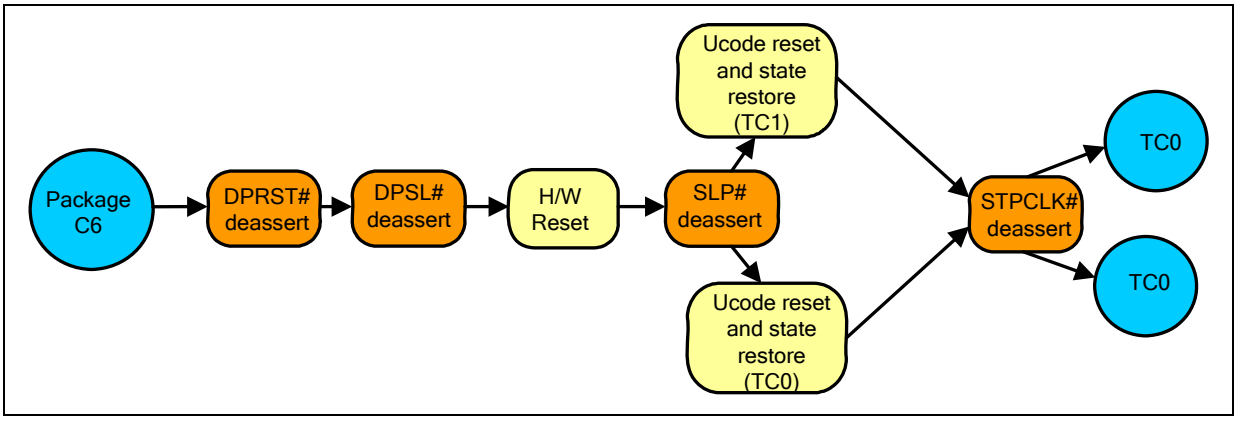
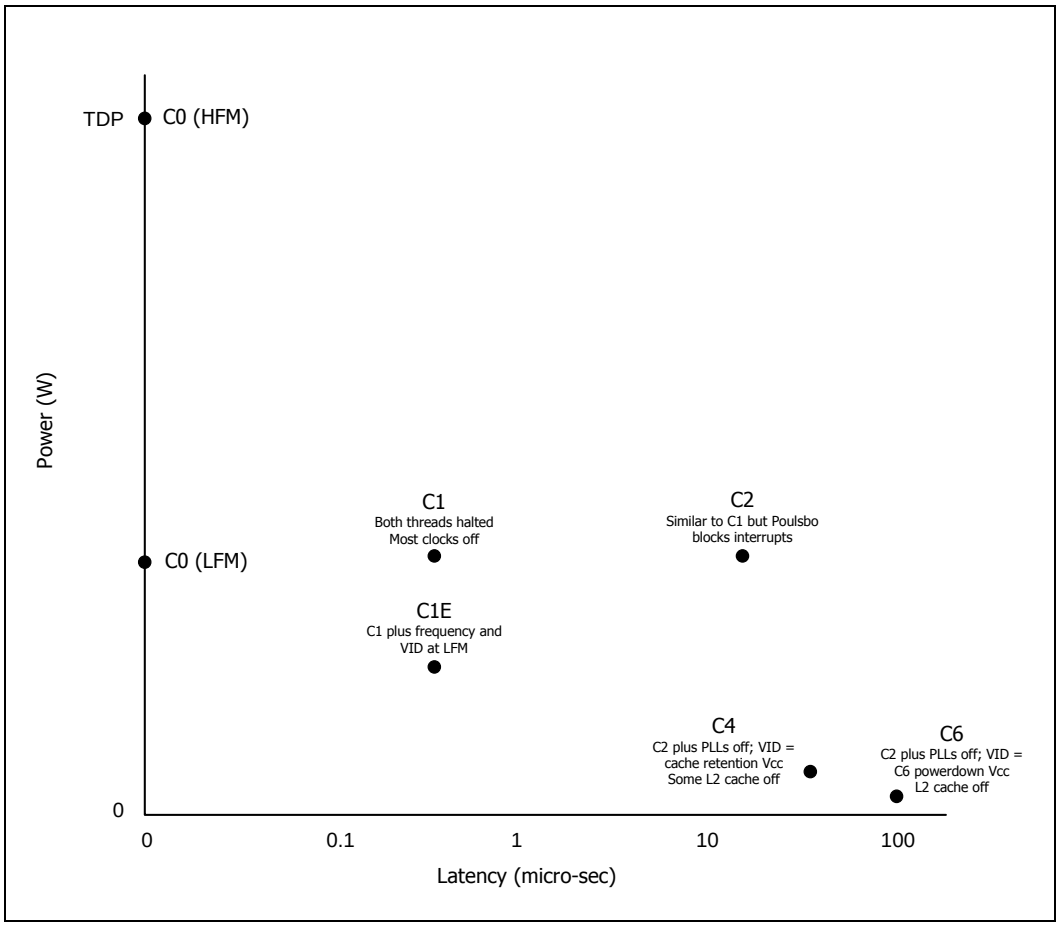


Figure 5 shows the relative exit latencies of the package sleep states discussed above. Note that this figure uses pre-silicon estimates. Silicon based data will be provided in a future revision of this document.

Figure 5. Exit Latency Table



2.2 Dynamic Cache Sizing

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following conditions:

- The C0 timer that tracks continuous residency in the Normal package state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The FSB speed to processor core speed ratio is below the predefined L2 shrink threshold.

The number of L2 cache ways disabled upon each Deeper Sleep entry is configured in the BBL_CR_CTL3 MSR. The C0 timer is referenced through the CLOCK_CORE_CST_CONTROL_STT MSR. The shrink threshold under which the L2 cache size is reduced is configured in the PMG_CST_CONFIG_CONTROL MSR. If the FSB speed to processor core speed ratio is above the predefined L2 shrink threshold, L2 cache expansion will be requested. If the ratio is zero, the ratio will not be taken into account for Dynamic Cache Sizing decisions.

Upon STPCLK# de-assertion, the core exiting Intel Enhanced Deeper Sleep state or C6 will expand the L2 cache to two ways and invalidate previously disabled cache ways. If the L2 cache reduction conditions stated above still exist when the core returns to C4 then package enters Intel Enhanced Deeper Sleep state or C6, then the L2 will be shrunk to zero again. If the core requests a processor performance state resulting in a higher ratio than the predefined L2 shrink threshold, the C0 timer expires, then the whole L2 will be expanded upon the next interrupt event.

In addition, the processor supports Full Shrink on L2 cache. When the MWAIT C6 instruction is executed with a hint=0x2 in ECX[3:0], the microcode will shrink all the active ways of the L2 cache in one step. This ensures that the package enters C6 immediately when it is in TC6 instead of iterating until the cache is reduced to zero. The operating system (OS) is expected to use this hint when it wants to enter the lowest power state and can tolerate the longer entry latency.

L2 cache shrink prevention may be enabled as needed on occasion through an MWAIT(C4) sub-state field. If shrink prevention is enabled, the processor does not enter Intel Deeper Sleep state (C6) since the L2 cache remains valid and in full size.

2.3 Enhanced Intel SpeedStep® Technology

The processor features Enhanced Intel SpeedStep® Technology. Following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple voltage and frequency operating points provide optimal performance at the lowest power.
- Voltage and frequency selection is software controlled by writing to processor MSRs:
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps by placing new values on the VID pins and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency and the V_{CC} is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition completes.
- The processor controls voltage ramp rates internally to ensure glitch free transitions.
- Low transition latency and large number of transitions possible per second:
  - Processor core (including L2 cache) is unavailable for up to 10 µs during the frequency transition.
  - The bus protocol (BNR# mechanism) is used to block snooping.
- Improved Intel® Thermal Monitor mode:
  - When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency and voltage specified in a software programmable MSR.
  - The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up transition to the previous frequency and voltage point occurs.
  - An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system level thermal management.
- Enhanced thermal management features:
  - Digital Thermal Sensor and Out of Specification detection
  - Intel Thermal Monitor 1 (TM1) in addition to Intel Thermal Monitor 2 (TM2) in case of unsuccessful TM2 transition.

2.4 Enhanced Low-Power States

Enhanced low-power states (C1E, C2E, C4E) optimize for power by forcibly reducing the performance state of the processor when it enters a package low-power state. Instead of directly transitioning into the package low-power state, the enhanced package low-power state first reduces the performance state of the processor by performing an Enhanced Intel SpeedStep® Technology transition down to the lowest operating point. Upon receiving a break event from the package low-power state, control is returned to software while an Enhanced Intel SpeedStep Technology transition up to the initial operating point occurs. The advantage of this feature is that it significantly reduces leakage while in the Stop-Grant and Deeper Sleep states.

Note: Long-term reliability cannot be assured unless all the Enhanced Low-Power States are enabled.

The processor implements two software interfaces for requesting enhanced package low-power states: MWAIT instruction extensions with sub-state hints and using BIOS by configuring IA32_MISC_ENABLES MSR bits to automatically promote package low-power states to enhanced package low-power states.

Caution: **Enhanced Stop-Grant and Enhanced Deeper Sleep must be enabled using the BIOS for the processor to remain within specification.** Not complying with this guideline may affect the long-term reliability of the processor.

Enhanced Intel SpeedStep Technology transitions are multi-step processes that require clocked control. These transitions cannot occur when the processor is in the Sleep or Deep Sleep package low-power states since processor clocks are not active in these states. Enhanced Deeper Sleep is an exception to this rule when the Hard C4E configuration is enabled in the IA32_MISC_ENABLES MSR. This Enhanced Deeper Sleep state configuration will lower core voltage to the Deeper Sleep level while in Deeper Sleep and, upon exit, will automatically transition to the lowest operating voltage and frequency to reduce snoop service latency. The transition to the lowest operating point or back to the original software requested point may not be instantaneous. Furthermore, upon very frequent transitions between active and idle states, the transitions may lag behind the idle state entry resulting in the processor either executing for a longer time at the lowest operating point or running idle at a high operating point. Observations and analyses show this behavior should not significantly impact total power savings or performance score while providing power benefits in most other cases.

2.5 FSB Low Power Enhancements

The processor incorporates FSB low power enhancements:

- BPRI# control for address and control input buffers
- Dynamic Bus Parking
- Dynamic On Die Termination disabling
- Low V_{CCP} (I/O termination voltage)
- Split V_{TT}
- CMOS Front Side Bus

The processor incorporates the DPWR# signal that controls the data bus input buffers on the processor. The DPWR# signal disables the buffers when not used and activates them only when data bus activity occurs. This results in significant power savings with no performance impact. BPRI# control also allows the processor address and control input buffers to be turned off when the BPRI# signal is inactive. Dynamic Bus Parking allows a reciprocal power reduction in chipset address and control input buffers when the processor de-asserts its BR0# pin. The On-Die Termination on the processor FSB buffers is disabled when the signals are driven low, resulting in additional power savings. The low I/O termination voltage is on a dedicated voltage plane independent of the core voltage, enabling low I/O switching power at all times.

2.5.1 Split V_{TT}

Split V_{TT} is an enhancement designed to support the C6 power state. As deeper ACPI C-states are reached, leakage power becomes the only remaining source of power in the processor core. The goal of C6 is to eliminate leakage power by completely removing voltage from the processor core. The goal is aided by the introduction of Split V_{TT}.

As the name Split V_{TT} implies, a motherboard using the processor may support a split V_{TT} rail. This split rail implementation will allow power to be removed from approximately 90% of the I/O pins while in C6. These pins are powered by one Split V_{TT} rail. The only pins that remain powered are those needed to awake from the C6 state. These pins are powered by the second Split V_{TT} rail. To enter this power saving mode (while in C6), the Intel SCH asserts SLPIOVR# which gates an external FET. This situation results in an approximately 30% reduction in leakage current used.

2.5.2 CMOS Front Side Bus

The processor has a hybrid signaling mode—where data and address busses run in CMOS mode and strobe signals operate in GTL mode. The reason to use GTL on strobe signals is to improve signal integrity. The implementation of a CMOS bus offers substantial power savings when compared with the traditional AGTL+ bus.

3 Electrical Specifications

This chapter contains signal group descriptions, absolute maximum ratings, voltage identification, and power sequencing. The chapter also includes DC specifications.

3.1 FSB, GTLREF, and CMREF

The processor supports two kinds of signalling protocol: Complementary Metal Oxide Semiconductor (CMOS) and Advanced Gunning Transceiver Logic (AGTL+).

The “CMOS FSB” terminology used in this document refers to a hybrid signaling mode where data and address busses run in CMOS mode and strobe signals operate in GTL mode. The reason to use GTL on strobe signals is to improve signal integrity.

The termination voltage level for the processor CMOS and AGTL+ signals is V_{CCP} = 1.05V (nominal). Due to speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families.

The CMOS data and address busses require a reference voltage (CMREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. CMREF is only applicable to data and address signals, not to the sideband signals listed in Table 5. CMREF must be generated on the system board. In CMOS mode, there is no receiver-side termination to I/O voltage (V_{CCP}).

The AGTL+ inputs, including the sideband signals listed in Table 5, require a reference voltage (GTLREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board. Termination resistors are provided on the processor silicon and are terminated to its I/O voltage (V_{CCP}). The appropriate chipset will also provide on-die termination, thus eliminating the need to terminate the bus on the system board for most AGTL+ signals.

The CMOS bus depends on reflected wave switching and the AGTL+ bus depends on incident wave switching. Timing calculations for CMOS and AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system.

3.2 Power and Ground Pins

For clean, on-chip power distribution, the processor will have a large number of VCC (power) and VSS (ground) inputs. All power pins must be connected to V_{CC} power planes while all VSS pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. The processor VCC pins must be supplied by the voltage determined by the VID (Voltage ID) pins.

3.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage, such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component (e.g., coming out of an idle condition). Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 7. Failure to do so can result in timing violations or reduced lifetime of the component.

3.3.1 V_{CC} Decoupling

V_{CC} regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low-power states, must be provided by the voltage regulator solution

3.3.2 FSB AGTL+ Decoupling

The processor integrates signal termination on the die. Decoupling must also be provided by the system motherboard for proper AGTL+ bus operation.

3.4 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier will be set at its default ratio at manufacturing. The processor uses a differential clocking implementation.

3.5 Voltage Identification and Power Sequencing

The processor uses seven voltage identification pins (VID[6:0]) to support automatic selection of power supply voltages. The VID pins for the processor are CMOS outputs driven by the processor VID circuitry. Table 3 specifies the voltage level corresponding to the state of VID[6:0]. A “1” refers to a high-voltage level and a “0” refers to low-voltage level.

Power source characteristics must be stable whenever the supply to the voltage regulator is stable.

Table 3. Voltage Identification Definition

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000

3.6 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125 °C (maximum), or if the THERMTRIP# signal is asserted, the V_{CC} supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted.

3.7 Reserved and Unused Pins

RSVD[3:0] must be tied directly to V_{CCP} (1.05 V) non C6 rail to ensure proper operation of the processor. All other RSVD signals can be left as No Connect. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected.

3.8 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip and the appropriate chipset on the platform. The BSEL encoding for BCLK[1:0] is shown in Table 4.

Table 4. BSEL[2:0] Encoding for BCLK Frequency

BSEL[2]	BSEL[1]	BSEL[0]	BCLK Frequency
L	L	H	133 MHz
H	L	H	100 MHz

NOTES: All other bus selections reserved.

3.9 FSB Signal Groups

To simplify the following discussion, the FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

Implementation of a source synchronous data bus necessitates the need to specify two sets of timing parameters. One set is for common clock signals, which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.), and the second set is for the source synchronous signals, which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 5 identifies which signals are; common clock, source synchronous, and asynchronous.

Table 5. FSB Pin Groups

Signal Group	Type	Signals1
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, PREQ#4, RESET#, RS[2:0]#, TRDY#, DPWR#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, BNR#, BPM[3:0]#, BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#
CMOS Source Synchronous I/O	Synchronous to assoc. strobe	**Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB0# A[31:17]# — ADSTB1# D[15:0]# — DSTBP0#, DSTBN0# D[31:16]# — DSTBP1#, DSTBN1# D[47:32]# — DSTBP2#, DSTBN2# D[63:48]# — DSTBP3#, DSTBN3# Strobes use AGTL signaling always; data pins are CMOS only.
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
CMOS Input	Asynchronous	DPRSTP#, DPSLP#, IGNNE#, INIT#, LINT0/INTR, LINT1/ NMI, PWRGOOD, SMI#, SLP#, STPCLK#
Open Drain Output	Asynchronous	FERR#, THERMTRIP#, IERR#
Open Drain I/O	Asynchronous	
CMOS Output	Asynchronous	VID[6:0], BSEL[2:0]
CMOS Input	Synchronous to TCK	TCK, TDI, TMS, TRST#

Signal Group	Type	Signals1
Open Drain Output	Synchronous to TCK	TDO
FSB Clock	Clock	BCLK[1:0]
Power/Other		COMP[3:0], HFPLL, CMREF, GTLREF, DCLK, ADK, THERMDA, THERMDC, VCC, VCCA, VCCP, VCC_SENSE, VSS, VSS_SENSE, VCCFUSE, VCCPC6

NOTES:

1. Refer to Chapter 4 for signal descriptions and termination requirements.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. PROCHOT# signal type is open drain output and CMOS input.
4. On die termination differs from other AGTL+ signals.

3.10 CMOS Asynchronous Signals

CMOS input signals are shown in Table 5. Legacy output FERR#, IERR#, and other non- AGTL+ signals (THERMTRIP# and PROCHOT#) use Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the CMOS signals are required to be asserted for more than 5 BCLKs for the processor to recognize them. See Section 3.12 for the DC specifications for the CMOS signal groups.

3.11 Test Access Port (TAP) Connection

3.11.1 Maximum Ratings

Table 6 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 6. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1]
$T_{STORAGE}$	Processor Storage Temperature	-40	85	°C	2,3,4
$V_{CC, VCCP, VCCPC6}$	Any Processor Supply Voltage with Respect to V_{SS}	-0.3	1.10	V	5
V_{CCA}	PLL power supply	-0.3	1.575	V	
VinAGTL+	AGTL+ Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.10	V	
VinAsynch_CMOS	CMOS Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.10	V	

NOTES:

1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long term reliability of the device. For functional operation, refer to the processor case temperature specifications.
3. This rating applies to the processor and does not include any tray or packaging.
4. Failure to adhere to this specification can affect the long term reliability of the processor.
5. The V_{CC} max supported by the process is 1.2 V but the parameter can change (burnin voltage is higher).

3.12 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Chapter 4 for the pin signal definitions and signal pin assignments. Most of the signals on the FSB are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 10. DC specifications for the CMOS group are listed in Table 11.

Table 10 through Table 12 list the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency Mode (HFM) and Lowest Frequency Mode (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states except in the Deep Sleep and Deeper Sleep states. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the processor are at T_J = 90° C. Care should be taken to read all notes associated with each parameter.

Table 7. Voltage and Current Specifications for Intel® Atom™ Processor Z540, Z530, Z520, and Z510

Symbol	Parameter		Min	Typ	Max	Unit	Notes[11]
FSB Frequency	BCLK Frequency		100.00	—	133.35	MHz	
V_{CC}HFM	V_{CC} at Highest Frequency Mode (HFM)		AVID	—	1.10	V	1, 2, 10
V_{CC}LFM	V_{CC} at Lowest Frequency Mode (LFM)		0.75	—	AVID	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.20	—	V	2, 6
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	12
V_{CCPC6}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	12
V_{CCA}	PLL Supply voltage		1.425	1.5	1.575	V	
$V_{CCDPPWDN}$	V_{CC} at Deep Power-Down Technology (C6)		0.30	0.35	0.40	V	13
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep (C4)		0.75	—	1.0	V	1, 2
V_{CCF}	Fuse Power Supply		1.00	1.05	1.10	V	
I_{CCDES}	I_{CC} for Processor Recommended Design Target (Estimated) for Z540		—	—	4.0	A	
I_{CCDES}	I_{CC} for Processors Recommended Design Target (Estimated) for Z530, Z520, Z510		—	—	3.5	A	
I_{CC}	Processor Number	Core Frequency/Voltage	—	—	—	—	—
	Z540	HFM: 1.86 GHz LFM: 0.80 GHz			3.2 1.5	A	3, 4
	Z530 Z520 Z510	HFM: 1.60 GHz LFM: 0.80 GHz HFM: 1.33 GHz LFM: 0.80 GHz HFM: 1.10 GHz LFM: 0.60 GHz	—	—	2.50 1.25 2.50 1.25 2.50 1.25	A	3, 4
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM: 1.1–1.86 GHz @ 1.10 Volts LFM: 0.6 – 0.8 GHz @ 0.85 Volts		— —	— —	2.0 1.3	A	3, 4
I_{DSLP}	I_{CC} Deep Sleep HFM: 1.1 – 1.86 GHz @ 1.10 Volts LFM: 0.6 – 0.8 GHz @ 0.85 Volts		— —	— —	1.2 0.4	A	At 50°C 3, 4
I_{DPRSLP}	I_{CC} Deeper Sleep (C4)		—	—	0.2	A	At 50°C 3, 4
$dI_{CC/dt}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin (Estimated)		—	—	2.5	A/µs	5, 7
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	

Symbol	Parameter	Min	Typ	Max	Unit	Notes[11]
I_{CCP}+ $I_{CCP}C6$	I_{CCP} + $I_{CCP}C6$ before V_{CC} Stable	—	—	2.5	A	8
I_{CCP}+ $I_{CCP}C6$	I_{CCP} + $I_{CCP}C6$ after V_{CC} Stable	—	—	1.5	A	9

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep® Technology, or Enhanced Halt State). Typical AVID range is 0.8V to 0.85V.
2. The voltage specifications are assumed to be measured across VCC_SENSE and VSS_SENSE pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 90 °C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance is shown in Figure 6 and Figure 7.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification, which is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification, which is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. The V_{CC} max supported by the process is 1.1V but the parameter can change (burnin voltage is higher).
11. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
12. V_{CCP} may be turned off during C6 power state; V_{CCPC6} must always be powered on to 1.05V ±5% on all power states.
13. The V_{CC} power supply needs to be set to 0.3 to 0.4V during C6 power state.

Table 8. Voltage and Current Specifications for Intel® Atom™ Processor Z500

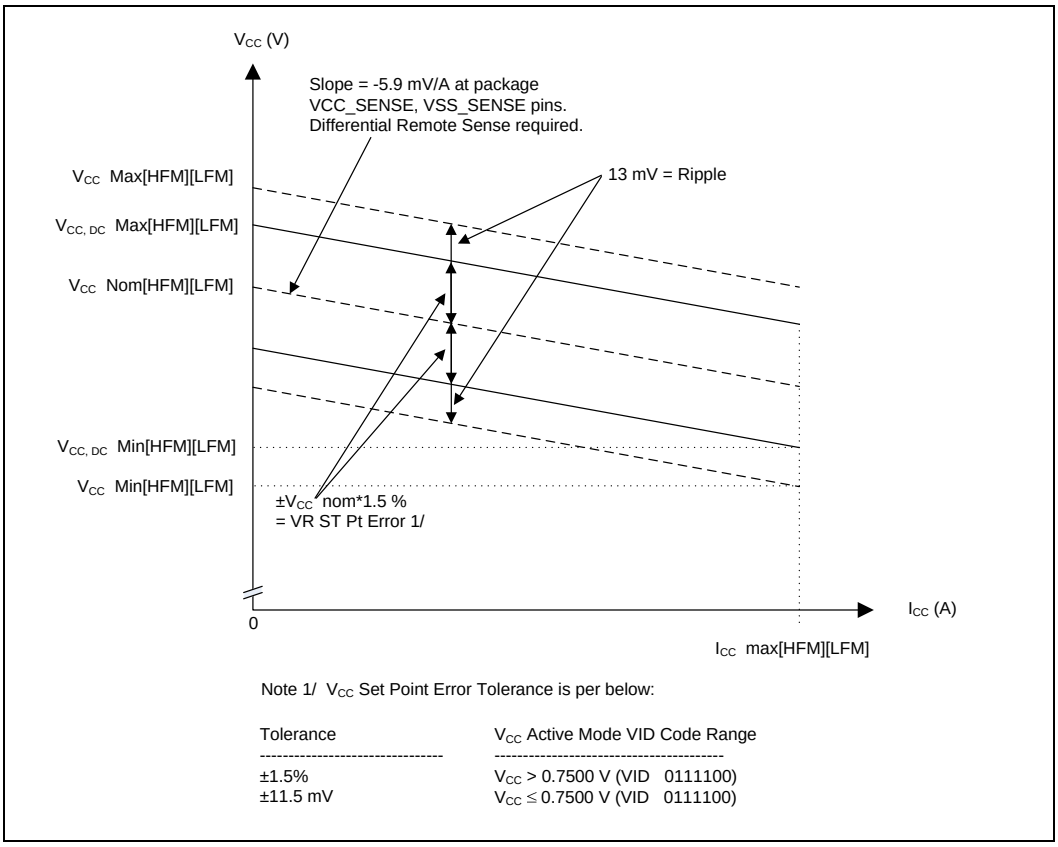
Symbol	Parameter		Min	Typ	Max	Unit	Notes[11]
FSB Frequency	BCLK Frequency		—	100.0	—	MHz	
V_{CC}HFM	V_{CC} at Highest Frequency Mode (HFM)		AVID	—	0.85	V	1, 2, 10
V_{CC}LFM	V_{CC} at Lowest Frequency Mode (LFM)		0.75	—	AVID	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power Up		—	1.10	—	V	2, 6
V_{CCP}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	12
V_{CCPC6}	AGTL+ Termination Voltage		1.00	1.05	1.10	V	12
V_{CCA}	PLL Supply Voltage		1.425	1.5	1.575	V	
$V_{CCDPPWDN}$	V_{CC} at Deep Power-Down Technology (C6)		0.30	0.35	0.40	V	13
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep (C4)		0.3	—	0.85	V	1, 2
I_{CCDES}	I_{CC} for Processor Recommended Design Target (Estimated)		—	—	2.0	A	
I_{CC}	Processor Number	Core Frequency/Voltage	—	—	—	—	—
	Z500	HFM: 0.8 GHz @ 0.85 Volts LFM: 0.6 GHz @ 0.75 Volts	—	—	0.8 0.6	A	3, 4
I_{AH}, I_{SGNT}	HFM: 0.8 GHz @ 0.85 Volts LFM: 0.6 GHz @ 0.75 Volts		—	—	0.7 0.5	A	3, 4
I_{DSLP}	I_{CC} Deep Sleep HFM: 0.8 GHz @ 0.85 Volts LFM: 0.6 GHz @ 0.75 Volts		—	—	0.20 0.13	A	At 50°C 3, 4
I_{DPRSLP}	I_{CC} Deeper Sleep (C4)		—	—	0.11	A	At 50°C 3, 4
$dI_{CC/dt}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin (Estimated)		—	—	2.5	A/µs	5, 7
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	
I_{CCP}+ I_{CCP}C6	I_{CCP} + I_{CCP}C6 before V_{CC} Stable		—	—	2.5	A	8
I_{CCP}+ I_{CCP}C6	I_{CCP} + I_{CCP}C6 after V_{CC} Stable		—	—	1.5	A	9

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State). Typical AVID range is 0.75V to 0.85V.
2. The voltage specifications are assumed to be measured across VCC_SENSE and VSS_SENSE pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.

3. Specified at 90°C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance is shown in Figure 6 and Figure 7.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification, which is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification, which is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. The V_{CC} max supported by the process is 1.1V but the parameter can change (burnin voltage is higher).
11. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
12. V_{CCP} may be turned off during C6 power state; V_{CCPC6} must always be powered on to 1.05V ±5% on all power states.
13. The V_{CC} power supply needs to be set to 0.3V to 0.4V during C6 power state.

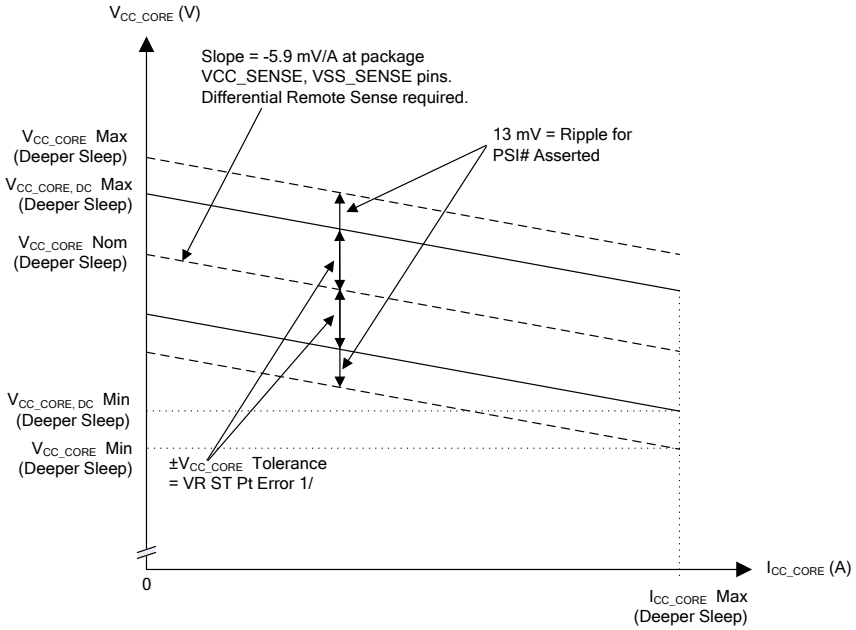
Figure 6. Active V_{CC} and I_{CC} Loadline



Note 1/ V_{CC} Set Point Error Tolerance is per below:

Tolerance	V_{CC} Active Mode VID Code Range
±1.5%	V_{CC} > 0.7500 V (VID 0111100)
±11.5 mV	$V_{CC} \leq$ 0.7500 V (VID 0111100)

Figure 7. Deeper Sleep V_{CC} and I_{CC} Loadline



Note 1/ Deeper Sleep VCC_CORE Set Point Error Tolerance is per below:

Tolerance - PSI# Ripple	V_{CC_CORE} VID Voltage Range
± [(VID*1.5%) - 3 mV]	V_{CC_CORE} > 0.7500 V
± (11.5 mV) - 3 mV]	0.7500 V £ V_{CC_CORE} £ 0.5000 V
± (25 mV) - 3 mV]	0.5000 V < V_{CC_CORE} £ 0.4125 V

Table 9. FSB Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes[1]
V_{IH}	Input High Voltage	—	—	1.15	V		7, 8
V_{IL}	Input Low Voltage	—	—	-0.3	V		7, 8
V_{CROSS}	Crossing Voltage	0.3	—	0.55	V		2, 7, 9
ΔV_{CROSS}	Range of Crossing Points	—	—	140	mV		2, 7, 5
V_{SWING}	Differential Output Swing	300	—	—	mV		6
I_{LI}	Input Leakage Current	-5	—	+5	µA		3
Cpad	Pad Capacitance	1.2	1.45	2.0	pF		4

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. For Vin between 0V and V_{IH}.
4. Cpad includes die capacitance only. No package parasitics are included.
5. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 2.
6. Measurement taken from differential waveform.
7. Measurement taken from single-ended waveform.
8. “Steady state” voltage, not including Overshoots or Undershoots.
9. Only applies to the differential rising edge (BCLK0 rising and BCLK1 falling).

Table 10. AGTL+ / CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	12
$V_{CCP}C6$	I/O Voltage for C6	1.00	1.05	1.10	V	12
GTLREF	GTL Reference Voltage	—	2/3 V_{CCP}	—	V	6
CMREF	CMOS Reference Voltage	—	1/2 V_{CCP}	—	V	6
R_{COMP}	Compensation Resistor	27.23	27.5	27.78	Ω	10
R_{ODT}	Termination Resistor	—	55	—	Ω	11
V_{IH}	Input High Voltage	GTLREF+0.10 or CMREF+0.10	V_{CCP}	V_{CCP}+0.10	V	3,6
V_{IL}	Input Low Voltage	-0.10	0	GTLREF–0.10 or CMREF–0.10	V	2,4
V_{OH}	Output High Voltage	V_{CCP}–0.10	V_{CCP}	V_{CCP}	V	6
R_{TT}	Termination Resistance	46 [SS] 46 [CC]	55	61 [SS] 64 [CC]	Ω	7, 13
R_{ON} (GTL mode)	GTL Buffer on Resistance	21	25	29	Ω	5
R_{ON} (CMOS mode)	CMOS Buffer on Resistance	42 [SS] 42 [CC]	50	55 [SS] 58 [CC]	Ω	5, 13
I_{LI}	Input Leakage Current	—	—	±100	µA	8
Cpad	Pad Capacitance	1.8	2.1	2.75	pF	9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull-down driver resistance. Measured at 0.31*V_{CCP}. R_{ON} (min) = 0.4*R_{TT}, R_{ON} (typ) = 0.455*R_{TT}, R_{ON} (max) = 0.51*R_{TT}. R_{TT} typical value of 55 Ω is used for R_{ON} typ/min/max calculations.
6. GTLREF and CMREF should be generated from V_{CCP} with a 1% tolerance resistor divider. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
7. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Measured at 0.31*V_{CCP}. R_{TT} is connected to V_{CCP} on die.
8. Specified with on die R_{TT} and R_{ON} are turned off. Vin between 0 and V_{CCP}.
9. Cpad includes die capacitance only. No package parasitics are included.
10. There are external resistors on the comp0 and comp2 pins.
11. On die termination resistance, measured at 0.33*V_{CCP}.
12. V_{CCP}=$V_{CCP}C6$ during normal operation. When in C6 state, V_{CCP}=0V while $V_{CCP}C6$=1.05 V.
13. SS: source synchronous pins such as quad-pumped data bus and double-pumped address bus which require a clock strobe. CC: Common clock pins.

Table 11. Legacy CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	8
$V_{CCP}C6$	I/O Voltage for C6	1.00	1.05	1.10	V	8
V_{IH}	Input High Voltage	$0.7*V_{CCP}$	V_{CCP}	VCCP+0.1	V	2
V_{IL}	Input Low Voltage CMOS	-0.10	0.00	$0.3*V_{CCP}$	V	2
V_{OH}	Output High Voltage	$0.9*V_{CCP}$	V_{CCP}	V_{CCP}+0.1	V	2
V_{OL}	Output Low Voltage	-0.10	0	$0.1*V_{CCP}$	V	2
I_{OH}	Output High Current	1.5	—	4.1	mA	4
I_{OL}	Output Low Current	1.5	—	4.1	mA	3
I_{LI}	Input Leakage Current	—	—	± 100	µA	5
Cpad1	Pad Capacitance	1.6	2.1	2.55	pF	6
Cpad2	Pad Capacitance for CMOS Input	0.95	1.2	1.45		7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCP} referred to in these specifications refers to instantaneous V_{CCP}.
3. Measured at $0.1*V_{CCP}$.
4. Measured at $0.9*V_{CCP}$.
5. For Vin between 0V and V_{CCP}. Measured when the driver is tri-stated.
6. Cpad1 includes die capacitance only for DPRSTP#, DPSLP#, PWRGOOD. No package parasitics are included.
7. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.
8. $V_{CCP}C6 = V_{CCP}$ during normal operation and a specific tolerance may be added for this later.

Table 12. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{OH}	Output High Voltage	V_{CCP}.–5%	V_{CCP}	V_{CCP}+5%	V	3
V_{OL}	Output Low Voltage	0	—	0.20	V	
I_{OL}	Output Low Current	16	—	50	mA	2
I_{LO}	Output Leakage Current	—	—	±200	µA	4
Cpad	Pad Capacitance	1.9	2.2	2.45	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V.
3. V_{OH} is determined by value of the external pull-up resistor to V_{CCP}.
4. For Vin between 0V and V_{OH}.
5. Cpad includes die capacitance only. No package parasitics are included.

3.13 AGTL+ FSB Specifications

Termination resistors are not required for most AGTL+ signals, as these are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers which compare a signal's voltage with a reference voltage called GTLREF (known as V_{REF} in previous documentation).

Table 11 lists the GTLREF and CMREF specifications. The AGTL+ and CMOS reference voltages (GTLREF and CMREF) should be generated on the system board using high precision voltage divider circuits. It is important that the system board impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well- controlled.

§

4 Package Mechanical Specifications and Pin Information

This chapter provides the package specifications, pinout assignments, and signal description.

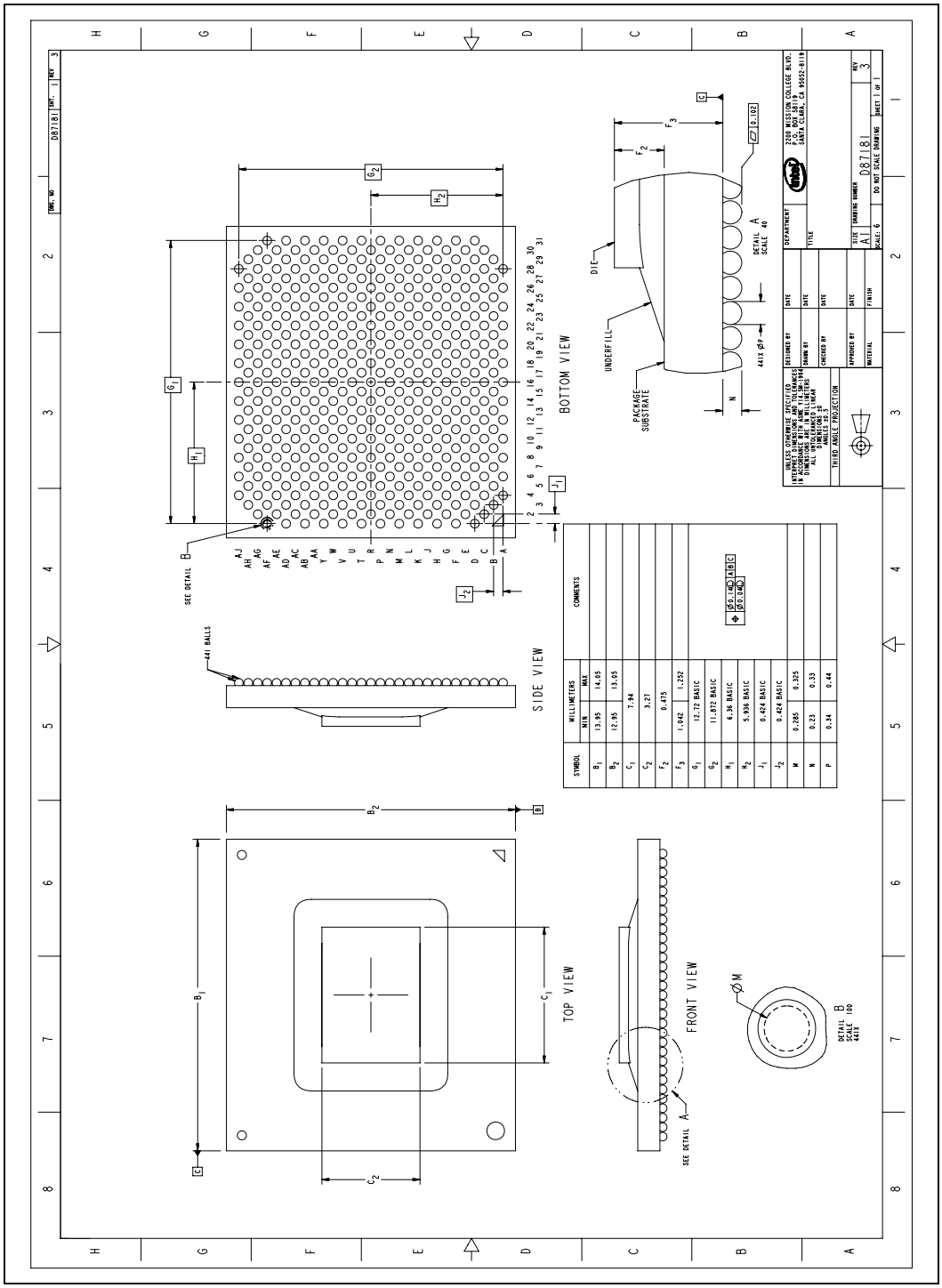
4.1 Package Mechanical Specifications

The processor will be available in 512 KB, 441 pins in FCBGA8 package. Figure 8 shows the package dimensions.

4.1.1 Processor Package Weight

The Intel Atom™ processor Z5xx series package weight is 0.475 g.

Figure 8. Package Mechanical Drawing



4.2 Processor Pinout Assignment

Figure 9 and Figure 10 are graphic representations of the processor pinout assignments. Table 13 lists the pinout by signal name.

Figure 9. Pinout Diagram (Top View, Left Side)

	AJ	AH	AG	AF	AE	AD	AC	AB	AA	Y	W	V	U	T	
1				VSS/NCTF		D[61]#		DSTBN[3]#		D[51]#		VSS		THERMTRIP#	1
2			VSS/NCTF		D[60]#		D[59]#		D[62]#		VCC		VID[6]		2
3		VSS/NCTF		D[54]#		VSS		VSS		VSS		VSS		VSS	3
4	VSS/NCTF		D[53]#		D[57]#		D[63]#		DSTBP[3]#		D[58]#		THRMDC		4
5		D[48]#		D[52]#		VSS		D[49]#		DINV[3]#		VSS		THRMDA	5
6	D[50]#		VSS		D[56]#		D[55]#		VSS		VSS		VCC		6
7		D[45]#		D[40]#		D[33]#		VCCP		VSS		VSS		VSS	7
8	D[46]#		VSS		D[32]#		VSS		VCCP		VCC		VCC		8
9		D[36]#		D[35]#		VSS		VCCP		VSS		VSS		VSS	9
10	D[47]#		VSS		D[37]#		VSS		VCCP		VCC		VCC		10
11		DSTBN[2]#		DSTBP[2]#		VSS		VCCP		VSS		VSS		VSS	11
12	D[44]#		VSS		DINV[2]#		VSS		VCCP		VCC		VCC		12
13		D[42]#		D[39]#		COMP[1]		VCCP		VSS		VSS		VSS	13
14	D[43]#		VSS		COMP[0]		VSS		VCCP		VCC		VCC		14
15		D[34]#		D[41]#		RSVD		VCCP		VSS		VSS		VSS	15
16	D[38]#		VSS		RSVD		VSS		VCCP		VCC		VCC		16
17		D[27]#		RSVD		RSVD		VCCP		VSS		VSS		VSS	17
18	D[30]#		VSS		D[26]#		VSS		VCCP		VCC		VCC		18
19		D[24]#		D[31]#		D[28]#		VCCP		VSS		VSS		VSS	19
20	D[18]#		VSS		D[19]#		VSS		VCCP		VCC		VCC		20
21		DSTBP[1]#		DSTBN[1]#		VSS		VCCP		VSS		VSS		VSS	21
22	D[20]#		VSS		DINV[1]#		VSS		VCCP		VCC		VCC		22
23		D[23]#		D[25]#		VSS		VCCP		VSS		VSS		VSS	23
24	D[29]#		VSS		D[16]#		D[17]#		VSS		VCC		VCC		24
25		D[22]#		D[21]#		VSS		D[14]#		VSS		VSS		VSS	25
26	GTLREF		VSS		CMREF		D[15]#		D[6]#		VCCP		VCCP		26
27		D[1]#		D[11]#		D[12]#		VSS		D[0]#		TEST3		VSS	27
28	VSS/NCTF		D[13]#		DINV[0]#		D[9]#		DSTBN[0]#		DRDY#		BSEL[2]		28
29		VSS/NCTF		D[5]#		VSS		VSS		VSS		VSS		VSS	29
30			VSS/NCTF		D[4]#		D[3]#		DSTBP[0]#		D[8]#		TEST4		30
31				VSS/NCTF		D[10]#		D[7]#		D[2]#		DPWR#		TEST2	31
	AJ	AH	AG	AF	AE	AD	AC	AB	AA	Y	W	V	U	T	

Figure 10. Pinout Diagram (Top View, Right Side)

	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1		TMS		TDO		STPCLK#		IERR#		BPM[0]#		VSS/NCTF				1
2	VID[5]		TDI		TCK		SLP#		DPRSTP#		BPM[1]#		VSS/NCTF			2
3		VSS		VSS		VSS		VSS		VSS		BPM[3]#		VSS/NCTF		3
4	VID[1]		VID[2]		VID[4]		TRST#		PWRGOOD		PRDY#		A[29]#		VSS/NCTF	4
5		VID[0]		RESET#		VID[3]		PROCHOT#		BPM[2]#		A[19]#		A[17]#		5
6	VCC		VCC		VSS		VSS		DPSLP#		RSVD		VSS		A[22]#	6
7		VSS		VSS		VSS		VCCPC6		PREQ#		RSVD		A[26]#		7
8	VCC		VCC		VCC		VCCPC6		VSS		RSVD		VSS		A[28]#	8
9		VSS		VSS		VSS		VCCPC6		VSS		RSVD		A[21]#		9
10	VCC		VCC		VCC		VCCP		VSS		RSVD		VSS		A[25]#	10
11		VSS		VSS		VSS		VCCP		VSS		ADSTB[1]#		A[31]#		11
12	VCC		VCC		VCC		VCCP		VSS		A[20]#		VSS		A[18]#	12
13		VSS		VSS		VSS		VCCP		VSS		A[27]#		A[23]#		13
14	VCC		VCC		VCC		VCCP		VSS		A[24]#		VSS		A[30]#	14
15		VSS		VSS		VSS		VCCP		COMP[3]		A[12]#		A[16]#		15
16	VCC		VCC		VCC		VCCP		VSS		COMP[2]		VSS		A[10]#	16
17		VSS		VSS		VSS		VCCP		VSS		A[15]#		A[7]#		17
18	VCC		VCC		VCC		VCCP		VSS		A[11]#		VSS		A[8]#	18
19		VSS		VSS		VSS		VCCP		VSS		ADSTB[0]#		A[13]#		19
20	VCC		VCC		VCC		VCCP		VSS		REQ[2]#		VSS		A[14]#	20
21		VSS		VSS		VSS		VCCP		VSS		A[5]#		REQ[4]#		21
22	VCC		VCC		VCC		VCCP		VSS		A[3]#		VSS		A[4]#	22
23		VSS		VSS		VSS		VCCP		VSS		REQ[1]#		A[9]#		23
24	VCC		VCC		VCC		VSS		BPRI#		A[6]#		VSS		REQ[3]#	24
25		VSS		VSS		VSS		BNR#		TRDY#		LOCK#		REQ[0]#		25
26	VCCP		VCCP		VCCP		SMI#		RSVD		RS[2]#		ADS#		RSVD	26
27		VSS		VCCPC6		RSVD		IGNNE#		VSS		RS[0]#		DEFER#		27
28	BCLK[1]		VSS		LINT1		FERR#		RSVD		RS[1]#		BR0#		VSS/NCTF	28
29		BCLK[0]		VSS		RSVD		VSS		HITM#		DBSY#		VSS/NCTF		29
30	BSEL[0]		VCCA		RSVD		RSVD		A20M#		HIT#		VSS/NCTF			30
31		TEST1		BSEL[1]		VSS		LINT0		INIT#		VSS/NCTF				31
	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Table 13. Pinout Arranged By Signal Name

Signal Name	Ball #
A[3]#	E22
A[4]#	A22
A[5]#	D21
A[6]#	E24
A[7]#	B17
A[8]#	A18
A[9]#	B23
A[10]#	A16
A[11]#	E18
A[12]#	D15
A[13]#	B19
A[14]#	A20
A[15]#	D17
A[16]#	B15
A[17]#	B5
A[18]#	A12
A[19]#	D5
A[20]#	E12
A[21]#	B9
A[22]#	A6
A[23]#	B13
A[24]#	E14
A[25]#	A10
A[26]#	B7
A[27]#	D13
A[28]#	A8
A[29]#	C4
A[30]#	A14
A[31]#	B11
A20M#	G30

Signal Name	Ball #
ADS#	C26
ADSTB[0]#	D19
ADSTB[1]#	D11
BCLK[0]	P29
BCLK[1]	R28
BNR#	H25
BPM[0]#	F1
BPM[1]#	E2
BPM[2]#	F5
BPM[3]#	D3
BPRI#	G24
BR0#	C28
RSVD	G26
BSEL[0]	R30
BSEL[1]	M31
BSEL[2]	U28
CMREF[1]	AE26
COMP[0]	AE14
COMP[1]	AD13
COMP[2]	E16
COMP[3]	F15
D[0]#	Y27
D[1]#	AH27
D[2]#	Y31
D[3]#	AC30
D[4]#	AE30
D[5]#	AF29
D[6]#	AA26
D[7]#	AB31
D[8]#	W30

Signal Name	Ball #
D[9]#	AC28
D[10]#	AD31
D[11]#	AF27
D[12]#	AD27
D[13]#	AG28
D[14]#	AB25
D[15]#	AC26
D[16]#	AE24
D[17]#	AC24
D[18]#	AJ20
D[19]#	AE20
D[20]#	AJ22
D[21]#	AF25
D[22]#	AH25
D[23]#	AH23
D[24]#	AH19
D[25]#	AF23
D[26]#	AE18
D[27]#	AH17
D[28]#	AD19
D[29]#	AJ24
D[30]#	AJ18
D[31]#	AF19
D[32]#	AE8
D[33]#	AD7
D[34]#	AH15
D[35]#	AF9
D[36]#	AH9
D[37]#	AE10
D[38]#	AJ16

Signal Name	Ball #
D[39]#	AF13
D[40]#	AF7
D[41]#	AF15
D[42]#	AH13
D[43]#	AJ14
D[44]#	AJ12
D[45]#	AH7
D[46]#	AJ8
D[47]#	AJ10
D[48]#	AH5
D[49]#	AB5
D[50]#	AJ6
D[51]#	Y1
D[52]#	AF5
D[53]#	AG4
D[54]#	AF3
D[55]#	AC6
D[56]#	AE6
D[57]#	AE4
D[58]#	W4
D[59]#	AC2
D[60]#	AE2
D[61]#	AD1
D[62]#	AA2
D[63]#	AC4
DBSY#	D29
DEFER#	B27
DINV[0]#	AE28
DINV[1]#	AE22
DINV[2]#	AE12
DINV[3]#	Y5

Signal Name	Ball #
DPRSTP#	G2
DPSLP#	G6
DPWR#	V31
DRDY#	W28
DSTBN[0]#	AA28
DSTBN[1]#	AF21
DSTBN[2]#	AH11
DSTBN[3]#	AB1
DSTBP[0]#	AA30
DSTBP[1]#	AH21
DSTBP[2]#	AF11
DSTBP[3]#	AA4
FERR#	J28
RSVD	G28
GTLREF	AJ26
HIT#	E30
HITM#	F29
IERR#	H1
IGNNE#	H27
INIT#	F31
LINT0	H31
LINT1	L28
LOCK#	D25
PRDY#	E4
PREQ#	F7
PROCHOT#	H5
PWRGOOD	G4
REQ[0]#	B25
REQ[1]#	D23
REQ[2]#	E20
REQ[3]#	A24

Signal Name	Ball #
REQ[4]#	B21
RESET#	M5
RS[0]#	D27
RS[1]#	E28
RS[2]#	E26
RSVD	K29
RSVD	D9
RSVD	D7
RSVD	E8
RSVD	E10
RSVD	L30
RSVD	J30
RSVD	E6
RSVD	AE16
RSVD	AF17
RSVD	AD15
RSVD	AD17
RSVD	A26
RSVD	K27
SLP#	J2
SMI#	J26
STPCLK#	K1
TCK	L2
TDI	N2
TDO	M1
TEST1	P31
TEST2	T31
TEST3	V27
TEST4	U30
THERMTRIP#	T1
THRMDA	T5

Signal Name	Ball #
THRMDC	U4
TMS	P1
TRDY#	F25
TRST#	J4
VCC	L8
VCC	L10
VCC	L12
VCC	L14
VCC	L16
VCC	L18
VCC	L20
VCC	L22
VCC	L24
VCC	N6
VCC	N8
VCC	N10
VCC	N12
VCC	N14
VCC	N16
VCC	N18
VCC	N20
VCC	N22
VCC	N24
VCC	R6
VCC	R8
VCC	R10
VCC	R12
VCC	R14
VCC	R16
VCC	R18
VCC	R20

Signal Name	Ball #
VCC	R22
VCC	R24
VCC	U6
VCC	U8
VCC	U10
VCC	U12
VCC	U14
VCC	U16
VCC	U18
VCC	U20
VCC	U22
VCC	U24
VCC	W8
VCC	W10
VCC	W12
VCC	W14
VCC	W16
VCC	W18
VCC	W20
VCC	W22
VCC	W24
VCCA	N30
VCCP	AA8
VCCP	AA10
VCCP	AA12
VCCP	AA16
VCCP	AA18
VCCP	AA20
VCCP	AA22
VCCP	AB7
VCCP	AB9

Signal Name	Ball #
VCCP	AB11
VCCP	AB13
VCCP	AB15
VCCP	AB17
VCCP	AB19
VCCP	AB21
VCCP	AB23
VCCP	H11
VCCP	H13
VCCP	H15
VCCP	H17
VCCP	H19
VCCP	H21
VCCP	H23
VCCP	J10
VCCP	J12
VCCP	J14
VCCP	J18
VCCP	J20
VCCP	J22
VCCP	L26
VCCP	N26
VCCP	R26
VCCP	U26
VCCP	W26
VCCP	AA14
VCCP	J16
VCCPC6	H7
VCCPC6	H9
VCCPC6	J8
VCCPC6	M27

Signal Name	Ball #
VCC_SENSE	W2
VID[0]	P5
VID[1]	R4
VID[2]	N4
VID[3]	K5
VID[4]	L4
VID[5]	R2
VID[6]	U2
VSS	K31
VSS / NCTF	A4
VSS / NCTF	A28
VSS	AA6
VSS	AA24
VSS	AB3
VSS	AB27
VSS	AB29
VSS	AC8
VSS	AC10
VSS	AC12
VSS	AC14
VSS	AC16
VSS	AC18
VSS	AC20
VSS	AC22
VSS	AD3
VSS	AD5
VSS	AD9
VSS	AD11
VSS	AD21
VSS	AD23
VSS	AD25

Signal Name	Ball #
VSS	AD29
VSS / NCTF	AF1
VSS / NCTF	AF31
VSS / NCTF	AG2
VSS	AG6
VSS	AG8
VSS	AG10
VSS	AG12
VSS	AG14
VSS	AG16
VSS	AG18
VSS	AG20
VSS	AG22
VSS	AG24
VSS	AG26
VSS / NCTF	AG30
VSS / NCTF	AH3
VSS / NCTF	AH29
VSS / NCTF	AJ4
VSS / NCTF	AJ28
VSS / NCTF	B3
VSS / NCTF	B29
VSS / NCTF	C2
VSS	C6
VSS	C8
VSS	C10
VSS	C12
VSS	C14
VSS	C16
VSS	C18
VSS	C20

Signal Name	Ball #
VSS	C22
VSS	C24
VSS / NCTF	C30
VSS / NCTF	D1
VSS / NCTF	D31
VSS	F3
VSS	F9
VSS	F11
VSS	F13
VSS	F17
VSS	F19
VSS	F21
VSS	F23
VSS	F27
VSS	G8
VSS	G10
VSS	G12
VSS	G14
VSS	G16
VSS	G18
VSS	G20
VSS	G22
VSS	H3
VSS	H29
VSS	J6
VSS	J24
VSS	K3
VSS	K7
VSS	K9
VSS	K11
VSS	K13

Signal Name	Ball #
VSS	K15
VSS	K17
VSS	K19
VSS	K21
VSS	K23
VSS	K25
VSS	L6
VSS	M3
VSS	M7
VSS	M9
VSS	M11
VSS	M13
VSS	M15
VSS	M17
VSS	M19
VSS	M21
VSS	M23
VSS	M25
VSS	M29
VSS	N28
VSS	P3
VSS	P7
VSS	P9
VSS	P11

Signal Name	Ball #
VSS	P13
VSS	P15
VSS	P17
VSS	P19
VSS	P21
VSS	P23
VSS	P25
VSS	P27
VSS	T3
VSS	T7
VSS	T9
VSS	T11
VSS	T13
VSS	T15
VSS	T17
VSS	T19
VSS	T21
VSS	T23
VSS	T25
VSS	T27
VSS	T29
VSS	V3
VSS	V5
VSS	V7

Signal Name	Ball #
VSS	V9
VSS	V11
VSS	V13
VSS	V15
VSS	V17
VSS	V19
VSS	V21
VSS	V23
VSS	V25
VSS	V29
VSS	W6
VSS	Y3
VSS	Y7
VSS	Y9
VSS	Y11
VSS	Y13
VSS	Y15
VSS	Y17
VSS	Y19
VSS	Y21
VSS	Y23
VSS	Y25
VSS	Y29
VSS_SENSE	V1

4.3 Signal Description

Table 14. Signal Description

Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) defines a 2^{32}-byte physical memory address space. In subphase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the processor FSB. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is de-asserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal loop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** — **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB[0]# A[31:17]# — ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing VCROSS.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Signal Name	Type	Description
BPM[0]#	O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all FSB agents. This includes debug or performance monitoring tools.
BPM[1]#	I/O	
BPM[2]#	O	
BPM[3]#	I/O	
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are compeleted and then releases the bus by de-asserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the processor (Symmetric Agent) and Intel SCH (High Priority Agent).
BSEL[2:0]	O	BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. Table 4 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The processor operates at 400-MHz or 533-MHz system bus frequency100-MHz or 133-MHz BCLK frequency, respectively).
COMP[3:0]	PWR	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** **Data Group — DSTBN#/DSTBP# — DINV#** D[15:0]# — 0 — 0 D[31:16]# — 1 — 1 D[47:32]# — 2 — 2 D[63:48]# — 3 — 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is de-asserted. This signal must connect the appropriate pins on both FSB agents.

Signal Name	Type	Description
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both FSB agents.
DINV[3:0]#	I	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. DINV[3:0]# assignment to data bus signals is shown below. **Bus Signal — Data Bus Signals** DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPRSTP#	I	DPRSTP# when asserted on the platform causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. To return to the Deep Sleep State, DPRSTP# must be de-asserted. DPRSTP# is driven by the Intel SCH device.
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. To return to the Sleep State, DPSLP# must be de-asserted. DPSLP# is driven by the Intel SCH device.
DPWR#	I	DPWR# is a control signal from the Intel SCH device used to reduce power on the processor data bus input buffers.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be de-asserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. **Signals — Associated Strobe** D[15:0]# — DINV[0]#, DSTBN[0]# D[31:16]# — DINV[1]#, DSTBN[1]# D[47:32]# — DINV[2]#, DSTBN[2]# D[63:48]# — DINV[3]#, DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. **Signals — Associated Strobe** D[15:0]# — DINV[0]#, DSTBP[0]# D[31:16]# — DINV[1]#, DSTBP[1]# D[47:32]# — DINV[2]#, DSTBP[2]# D[63:48]# — DINV[3]#, DSTBP[3]#

Signal Name	Type	Description
FERR#/PBE#	O	FERR# (Floating-point Error) / PBE#(Pending Break Event) is a multiplexed signal pin and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*– type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is de-asserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* and the *Intel® Processor Identification and CPUID Instruction Application Note*.
CMREF	PWR	CMREF determines the signal reference level for CMOS input pins. CMREF should be set at 1/2 V_{CCP}. CMREF is used by the CMOS receivers to determine if a signal is a logical 0 or logical 1. If not using CMOS, then all CMREF and GTLREF should be provided with 2/3 V_{CCP}.
GTLREF	PWR	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# HITM#	I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET# or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is de-asserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, the processor reverses its FSB data and address signals internally to ease mother board layout for systems where the chipset is on the other side of the mother board. D[63:0] => D[0:63] A[31:3] => A[3:31] DINV[3:0]# is also reversed.
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	Probe Ready signal used by debug tools to determine processor debug readiness.
PRDY#	O	Probe Request signal used by debug tools to request debug operation of the processor.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	I/O, O (DP)	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#. This signal may require voltage translation on the motherboard.

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will de-assert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is de-asserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved	RSVD[3:0] pins E10, E8, D7, and D9 **must** be tied directly to V_{CCP} to ensure proper operation of the processor. All other RSVD signals can be left as No Connects.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, de-assertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is de-asserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the de-assertion of RESET# the processor will tri-state its outputs.

Signal Name	Type	Description
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units, except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is de-asserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST[1:4]		Test Signals. All TEST signals can be left as No Connects.
THRMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125 °C. This condition is signaled to the system by the THERMTRIP# (Thermal Trip) pin.
THRMDA	PWR	Thermal Diode - Anode
THRMDC	PWR	Thermal Diode - Cathode
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
VCCA	PWR	VCCA provides isolated power for the internal processor core PLLs.
VCC	PWR	Processor core power supply
VSS	GND	Processor core ground node.
VSS / NCTF	GND	Non Critical to Function

Signal Name	Type	Description
VID[6:0]	O	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). Unlike some previous generations of processors, these are CMOS signals that are driven by the processor. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 3 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
VCCP	PWR	Processor I/O Power Supply which needs to turn off in Deep Power-Down Technology (C6) state if Split V_{TT} is incorporated.
VCCPC6	PWR	Processor I/O Power Supply which needs to remain on in Deep Power-Down Technology (C6) state.
VCC_SENSE	O	VCC_SENSE is an isolated low impedance connection to processor core power (V_{cc}). It can be used to sense or measure power near the silicon with little noise
VSS_SENSE	O	VSS_SENSE is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise.

§

5 Thermal Specifications and Design Considerations

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section 5.1. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment enables long-term system operation. A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions include active or passive heat spreaders or heat exchangers attached to the exposed processor die. The solution should make firm contact to the die while maintaining processor mechanical specifications such as pressure. A typical system level thermal solution may consist of a system fan used to evacuate or pull air through the system in conjunction with a multi- component heat spreader used to reduce the temperature of the processor and other components while maintaining as uniform a skin temperature as possible. Alternatively, the processor may be in a fan-less system, but would likely still use a multi-component heat spreader. Note that trading of thermal solutions also involves trading performance.

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature (T_J) specifications at the corresponding thermal design power (TDP) value listed in Table 15 and Table 16. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The maximum junction temperature is defined by an activation of the processor Intel Thermal Monitor. Refer to Section 5.1.2 for more details. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 15 and Table 16. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 5.1.2. In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

Table 15. Power Specifications for Intel® Atom™ Processor Z540, Z530, Z520, and Z510

Symbol	Processor Number	Core Frequency and Voltage	Thermal Design Power	Unit	Notes
TDP	Z510	1.1 GHz & HFM V_{CC} 0.6 GHz & LFM V_{CC}	2.0 W	W	At 90°C 1, 4
	Z520	1.33 GHz & HFM V_{CC} 0.8 GHz & LFM V_{CC}	2.0 W 2.2 W with HT enabled	W	At 90°C 1, 4,6
	Z530	1.60 GHz & HFM V_{CC} 0.8 GHz & LFM V_{CC}	2.0 W 2.2 W with HT enabled	W	At 90°C 1, 4,6
	Z540	1.86 GHz & HFM V_{CC} 0.8 GHz & LFM V_{CC}	2.4 W 2.64 W with HT enabled	W	At 90°C 1, 4,6

Symbol	Parameter	Min	Typ	Max	Unit	Notes
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at HFM V_{CC} at LFM V_{CC}	—	—	 1.0 0.7	 W W	At 70°C 2
P_{DSLP}	Deep Sleep Power	—	—	0.5	W	At 50°C 2, 5
P_{DPRSLP}	Deeper Sleep Power	—	—	0.5	W	At 50°C 2, 5
P_{DC6}	Deep Power-Down Technology (C6)	—	—	0.1	W	At 50°C 2
T_J	Junction Temperature	0	—	90	°C	3, 4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Deep Sleep state is mapped to Deeper Sleep State.
6. Hyper-Threading Technology (HT Technology) requires a computer system with an Intel processor supporting Hyper-Threading Technology and an HT Technology enabled chipset, BIOS and operating system. Hyper-Threading Technology is available on select Intel® Atom™ processor components (Z520=1.33 GHz, Z530=1.60 GHz and Z540=1.86 GHz). HT Technology can add 200 mW of power above TDP, so 1.33 GHz and 1.6 GHz processor can have 2.2 W power and 1.86 GHz processor can have 2.64 W power when multi-threaded applications are run.

Table 16. Power Specifications for Intel® Atom™ Processor Z500

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	Z500 Z500	0.8 GHz & HFM V_{CC} 0.6 GHz & LFM V_{CC}	0.65			W	At 90°C 1, 4
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
PAH, PSGNT	Auto Halt, Stop Grant Power at HFM V_{CC} at LFM V_{CC}		—	—	0.6 0.5	W W	At 70°C 2
PDSLP	Deep Sleep Power		—	—	0.3	W	At 50°C 2, 5
PDPRSLP	Deeper Sleep Power		—	—	0.3	W	2, 5
PDC6	Deep Power-Down Technology (C6)		—	—	0.08	W	2
TJ	Junction Temperature		0	—	90	°C	3, 4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Deep Sleep state is mapped to Deeper Sleep State.

5.1 Thermal Specifications

The processor incorporates three methods of monitoring die temperature: the Digital Thermal Sensor, Intel Thermal Monitor, and the Thermal Diode. The Intel Thermal Monitor (detailed in Section 5.1.2) must be used to determine when the maximum specified processor junction temperature has been reached.

5.1.1 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal "diode", with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor MSR and applied. See Section 5.1.2 for more details. See Section 5.1.3 for thermal diode usage recommendation when the PROCHOT# signal is not asserted.

The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode T_{offset} value programmed into the processor Model Specific Register (MSR).

Table 17 and Table 18 provide the diode interface and specifications. Transistor model parameters shown in Table 18 provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Contact your external sensor supplier for their recommendation. The thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 17. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	T5	Thermal diode anode
THERMDC	U4	Thermal diode cathode

Table 18. Thermal Diode Parameters using Transistor Model

Symbol	Parameter	Min	Typ	Max	Unit	Notes
IFW	Forward Bias Current	5	—	200	µA	1
IE	Emitter Current	5	—	200	µA	1
nQ	Transistor Ideality	0.997	1.001	1.015		2,3,4
Beta		0.25	—	0.65		2,3
R_T	Series Resistance	2.79	4.52	6.24	Ω	2,5

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50–100 °C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_QkT} - 1)$$

   where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).

5. The series resistance, R_T, provided in the Diode Model Table (Table 18) can be used for more accurate readings, as needed.

When calculating a temperature based on the thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equation listed under Table 18. In most sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality value (also called n_{trim}) will be 1.000. Given that most diodes are not perfect, the designers usually select an n_{trim} value that more closely matches the behavior of the diodes in the processor. If the processor diode ideality deviates from that of the n_{trim}, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = Tmeasured * (1 - n_{actual}/n_{trim})$$

where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, n_{actual} is the measured ideality of the diode, and n_{trim} is the diode ideality assumed by the temperature sensing device.

5.1.2 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep Technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There are two automatic modes called Intel Thermal Monitor 1 (TM1) and Intel Thermal Monitor 2 (TM2). These modes are selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 and TM2 be enabled on the processor.

When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

When TM2 is enabled and a high temperature situation exists, the processor will perform an Enhanced Intel SpeedStep Technology transition to the LFM. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel SpeedStep Technology transition to the last requested operating point. The processor also supports Enhanced Multi Threaded Thermal Monitoring (EMTTM). EMTTM is a processor feature that enhances TM2 with a processor throttling algorithm known as Adaptive TM2. Adaptive TM2 transitions to intermediate operating points, rather than directly to the LFM, once the processor has reached its thermal limit and subsequently searches for the highest possible operating point. Ensure this feature is

enabled and supported in the BIOS. **Also with EMTTM enabled, the operating system can request the processor to throttling to any point between Intel Dynamic Acceleration frequency and Super LFM frequency as long as these features are enabled in the BIOS and supported by the processor.**

The Intel Thermal Monitor automatic mode and Enhanced Multi Threaded Thermal Monitoring must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 and TM2 be enabled on the processors.

TM1, TM2, and EMTTM features are collectively referred to as Adaptive Thermal Monitoring features.

TM1 and TM2 can co-exist within the processor. If both TM1 and TM2 bits are enabled in the auto-throttle MSR, TM2 will take precedence over TM1. However, if Force TM1 over TM2 is enabled in MSRs using BIOS and TM2 is not sufficient to cool the processor below the maximum operating temperature, then TM1 will also activate to help cool down the processor.

If a processor load based Enhanced Intel SpeedStep Technology transition (through MSR write) is initiated when a TM2 period is active, there are two possible results:

- If the processor load based Enhanced Intel SpeedStep Technology transition target frequency is **higher** than the TM2 transition based target frequency, the processor load-based transition will be deferred until the TM2 event has been completed.
- If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is **lower** than the TM2 transition based target frequency, the processor will transition to the processor load-based Enhanced Intel SpeedStep Technology target frequency point.

The TCC may also be activated using on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable using bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled; however, if the system tries to enable the TCC using on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, Deep Sleep, and Deeper Sleep low power states; hence, the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum

specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125 °C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

5.1.3 Digital Thermal Sensor

The processor also contains an on die Digital Thermal Sensor (DTS) that is read using an MSR (no I/O interface). The processor has a unique digital thermal sensor that's temperature is accessible using the processor MSRs. The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation using the Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (the Normal package level low power state).

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (T_{J_max}). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below T_{J_max}. Catastrophic temperature conditions are detectable using an Out Of Spec status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the "Out of Spec" status bit is set.

The DTS-relative temperature readout corresponds to the Thermal Monitor (TM1/TM2) trigger point. When the DTS indicates maximum processor core temperature has been reached, the TM1 or TM2 hardware thermal control mechanism will activate. The DTS and TM1/TM2 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient from the the core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach, and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected using two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts using the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

5.1.4 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's TM1 or TM2 are triggered and the temperature remains high, an "Out Of Spec" status and sticky bit are latched in the status MSR register and generates thermal interrupt.

5.1.5 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 or TM2 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals*.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC using PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When the core's thermal sensor trips, the PROCHOT# signal will be driven by the processor package. If only TM1 is enabled, PROCHOT# will be asserted and only the core that is above TCC temperature trip point will have its core clocks modulated. If TM2 is enabled and the core is above TCC temperature trip point, it will enter the lowest programmed TM2 performance state. It is important to note that Intel recommends both TM1 and TM2 to be enabled.

When PROCHOT# is driven by an external agent, if only TM1 is enabled on the core, then the processor core will have the clocks modulated. If TM2 is enabled, then the processor core will enter the lowest programmed TM2 performance state. It should be noted that Force TM1 on TM2, enabled using BIOS, does not have any effect on external PROCHOT#. If PROCHOT# is driven by an external agent when TM1, TM2, and Force TM1 on TM2 are all enabled, then the processor will still apply only TM2.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

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